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A Cost-Effective Fluorination Method for Enhancing the Performance of Metal Oxide Thin-Film Transistors Using a Fluorinated Planarization Layer

Sunbin Deng[1], Wei Zhong[1,3], Shou-Cheng Dong[1,2], Rongsheng Chen[1,3], Guijun Li[1,4], Meng Zhang[1,5], Fion Sze Yan Yeung[1], Man Wong[1], Hoi-Sing Kwok[1]

[1]State Key Laboratory of Advanced Displays and Optoelectronics Technologies, Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong

[2]Institute for Advanced Study, The Hong Kong University of Science and Technology, Hong Kong
[3]School of Microelectronics, South China University of Technology, Guangzhou, China
[4]College of physics and Optoelectronic Engineering, Shenzhen University, Shenzhen, China
[5]Institute of Microscale Optoelectronics, Shenzhen University, Shenzhen, China

Abstract

This work reports a fluorination method for metal oxide thin-film transistors through a planarization process using fluorinated polyimides. The fluorine diffusion from the planarization layer to the channels enhances device performance and reduces process thermal budget. This method is useful for the cost-effective production of active-matrix flat-panel display panels.

Author Keywords

Metal oxide; thin-film transistor; planarization; fluorination.

1. Introduction

Metal oxide (MO) thin-film transistors (TFTs) have become one of the mainstream backplane technologies in active-matrix flat-panel displays (AM-FPDs). However, their instabilities against electrical, thermal, and illumination stresses remain a critical issue. These instabilities are associated with various factors, one of which is oxygen-related deficiencies in MO channels [1], such as oxygen vacancies and weakly bonded oxygens.

To passivate these deficiencies, thermal annealing in oxygen (O)-containing atmospheres (i.e., oxidation) is a common practice in the fabrication of MO TFTs. However, these oxidation processes are usually performed at 300 °C or higher for hours, leading to a high thermal budget. This is undesirable in the pursuit of cost-effective manufacturing. Although annealing in O-rich gases, such as wet O_2 [2] and O_3 [3], or using alternative annealing techniques, such as high pressure [4], microwaves [5], and irradiation [6], can reduce the thermal budget to a limited extent, the requirement of additional facility and material costs makes these solutions economically unattractive.

Compared to oxidation, fluorination is a more efficient method to passivate oxygen-related deficiencies because fluorine has the largest electronegativity among all elements. In practice, fluorination is usually realized by a fluorine (F)-containing plasma treatment on MO channels [7]. It requires extra processing steps that have to be inserted in the process flow of MO TFTs, increasing manufacturing costs and prolonging production cycles. Additionally, ion bombardments during the plasma treatment often bring about undesirable device deterioration.

In this work, we develop a method to achieve fluorination of MO TFTs under mild conditions. By adopting a fluorinated polyimide (F-PI) in the planarization (PLN) process, a must-have step in the fabrication of AM-FPD panels, MO TFTs show improved electrical characteristics and stability, even when all thermal annealing steps before the PLN process were eliminated. This method is useful for the cost-effective production of AM-FPD panels and the implementation of MO TFTs on flexible substrates.

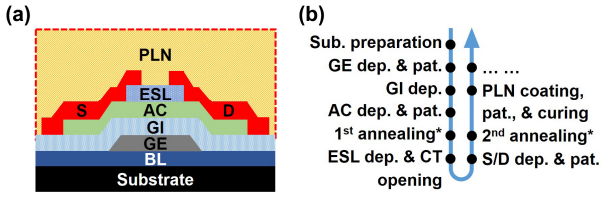

Figure 1. (a) Schematic diagram of the bottom-gated MO TFT with an ES layer and a PLN layer in this work. (b) Process flow of the MO TFTs in (a). The abbreviations of "dep.", "pat.", and "sub." are short for deposition, patterning, and substrate, respectively. The star (*) symbol indicates an optional step in the process flow.

2. Fabrication Processes

As shown in Fig. 1, the MO TFTs in this study adopt a bottom-gated architecture with an etch-stop (ES) layer and a PLN layer. The process flow started from 4-inch glass wafer. After wafer cleaning and SiO_2 buffer layer (BL) deposition, an Al/Mo bilayer was sputtered and patterned as gate electrodes (GEs). Then, a Si_3N_4 (50 nm) plus SiO_2 (75 nm) stack were deposited as gate insulator (GI) using plasma-enhanced chemical vapor deposition (PECVD). The equivalent oxide thickness (EOT) was 100 nm. Atop the GI stack, a layer of hybrid-phase indium tin oxide (ITO)-stabilized ZnO (50 nm) was sputtered and etched to form active channel (AC) islands. The detailed sputtering and wet etching processes are available in [8]. After the first thermal annealing at 300 °C in air for 2 hours, the ACs were capped by a 300-nm-thick PECVD SiO_2 ESL. Next, contact holes (CTs) were opened using reactive ion etching (RIE) in CHF_3 plasma and covered by 150-nm-thick Al pads, which served as source/drain (S/D) and gate testing pads. The devices were subjected to a second thermal annealing under the same condition as the first annealing. Lastly, a photosensitive F-PI was spin-coated on the devices, patterned by photolithography to expose the testing pads, and cured at 300 °C in air for 2 hours to form the PLN layer. For reference, we also prepared a control device with a non-fluorinated polyimide (NF-PI) PLN layer by following the above process flow. However, with no special statement, the PLN process in this paper generally refers to those steps using the F-PI. We denote the MO TFTs with the F-PI and the NF-PI PLN layer as Devices F1 and NF1, respectively. If the two annealing steps before the PLN process are removed, Devices F1 and NF1 will be further labeled as Devices F0 and NF0, respectively.

The electrical characteristics of these devices were measured in a dark probe station using a semiconductor parameter analyzer (B1500, Keysight). The device surface was profiled by atomic force microscopy (AFM, Park XE150S). A time-of-flight

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secondary ion mass spectrometry (TOF-SIMS, Physical Electronics PHI 7200) was employed to analyze the depth profiles of elements in different devices.

3. Results and Discussion

Fig. 2(a)-(c) show the AFM images and cross-sectional profiles of the MO TFT before and after the PLN process. The S/D-to-substrate height difference, which is the maximum across the device, can dramatically reduce from 423 nm to 158 nm by capping the ~2-µm-thick F-PI layer. The electrical strength of the F-PI PLN layer was then examined. To avoid high-voltage measurement, the PLN layer was thinned to a half of the normal thickness (~1 µm) and sandwiched between a heavily n-type doped (N++) Si wafer and an Al pad (800 µm×400 µm). At an applied bias of 100 V, the F-PI film show a leakage current density of ~10^{-7} A/cm^2. These results indicate that F-PI has good planarization and insulation properties and are suitable for display applications.

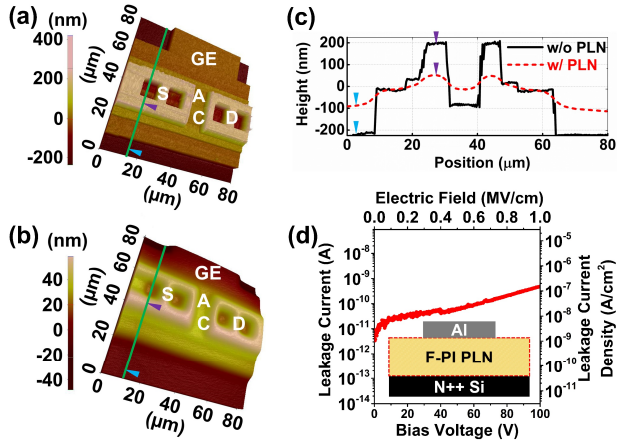

Figure 2. AFM image of the MO TFT (a) before and (b) after the PLN process. (c) Cross-sectional profiles along the green line in (a) and (b). The x-axis position is adjusted for well overlapping. (d) I-V characteristics of the F-PI PLN layer which is sandwiched by a N++ Si wafer and an Al pad.

In addition to satisfactory planarization and insulation efficacy, the PLN process also brings about performance enhancement to the MO TFTs. Fig. 3(a) shows the influence of the PLN process on the transfer curves of Device F1. With the cured F-PI layer, the device exhibits improved electrical characteristics with a positive shift of threshold voltage (V_{th}) from -3.3 V to -0.7 V, a decrease of subthreshold swing (SS) from 130.2 mV/decade to 80.8 mV/decade, and a rise of on-off ratio from 1.2×10^8 to 4.1×10^9. The clockwise hysteresis phenomenon observed before the PLN process almost disappears. In comparison, such a phenomenon continues with a hysteresis voltage of ~0.1 V in the control device if only the thermal curing step of the PLN process is performed. It indicates the deficiencies in the MO channel and at the GI/AC interface have not been sufficiently passivated. In other words, the PLN process is more effective in passivating deficiencies and improving device performance than conventional thermal annealing procedures.

Aided by the high-efficiency PLN process, we further fabricated Device F0 with a lower thermal budget. Its process flow followed that of Device F1 but with the first and second annealing steps skipped. The transfer curve of Device F0 is plotted in Fig. 3(b). Compared to Device F1, Device F0 shows no hysteresis and has a comparable V_{th} and SS of -0.8 V and 81.6 mV/decade, respectively. Probably due to the elimination of the additional annealing processes [9], the device owns relatively better S/D contacts with no current crowding effect in its output curves (Fig. 3(c)), leading to a higher on-off ratio of 1.5×10^{10} and a boosted saturation mobility (μ_{sat}) of 22.3 cm^2/Vs. The significant thermal budget reduction does not degrade the device uniformity in electrical performance across a large area. Fig. 3(d) plots the transfer curves of ten samples selected from the top, bottom, left, right, and center of a 4-inch glass wafer. All curves overlap well. Their μ_{sat}, V_{th}, and SS fluctuate in narrow ranges between 16 cm^2/Vs and 23 cm^2/Vs, -0.7 V and -0.9 V, and 75 mV/dec and 90 mV/dec, respectively, with relative standard deviations (RSDs) of 15.9%, 8.0%, and 5.2%, respectively.

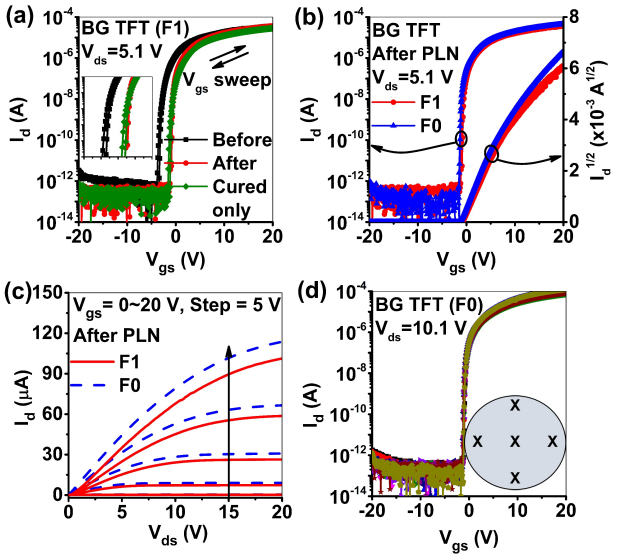

Figure 3. (a) Transfer curves of Device F1 before and after the PLN process. Comparison of (b) transfer curves and (c) output curves of Devices F1 and F0 after the PLN process. (d) Transfer curves of ten samples of Device F0 selected from the top, bottom, left, right, and center of a 4-inch glass wafer. The inset illustrates the selected positions, and there are two samples chosen for measurement at each position.

To elucidate the performance enhancement obtained by the PLN process, we analyzed the chemical composition of Devices F0 and NF0 before and after the PLN process by TOF-SIMS. The detection path starts from the PLN (if any), through the ESL and the AC, to the GI stack. All the signals are calibrated by employing the relatively stable O^- signal as a reference. The depth profiles of F^-, C^-, Si^- and ZnO^- along the path are shown in Fig. 4(a)-(d).

In all devices, the distribution and concentration of most species inside the AC are similar, except for F^- and C^-. As a result of the PLN process using the F-PI, the signal intensity of F^- and C^- near the GI/AC interface of Device F0 is significantly increased by about one and two orders of magnitude, respectively. Notably, the profile of F^- closely tracks that of C^- across all the layers of Device F0 after the PLN process, as shown in Fig. 5(c). This strongly indicates that the increased fluorine and carbon in the AC originated from the fluorinated PLN. During the thermal curing step, fragments such as CF_x radicals may be generated in the PLN under heat and then diffuse through the ES, which consists of low-density PECVD SiO_2, and eventually incorporated into the AC

bulk. The added fluorine contents may function as efficient agents to passivate oxygen-related deficiencies in MO channels considering that fluorine has the largest electronegativity (3.98) among elements [10]. The incorporated carbon has little positive impact on device performance, as evidenced in Fig. 4(d)-(f). There is also a diffusion of carbon from the non-fluorinated PLN to the AC bulk in Device NF0, but the device behaves much worse than Device F0 and Device N (i.e., the control device that only underwent the thermal curing in the PLN process).

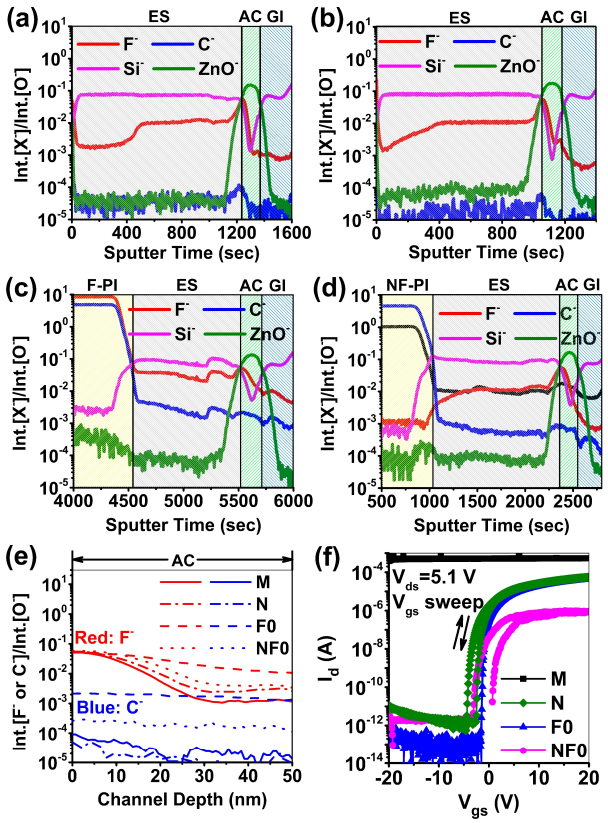

Figure 4. Depth profiles of X^- (= F^-, C^-, Si^-, ZnO^-) in (a) Device M (i.e., Device F0 or NF0 before the PLN process), (b) Device N (i.e., Device F0 or NF0 without the covering of the PLN layer but with the thermal curing step), (c) Device F0 after the PLN process, and (d) Device NF0 after the PLN process. (e) Expanded depth profiles of F^- and C^- in the AC layer of Devices M, N, F0, and NF0. (f) Transfer curves of Devices M, N, F0, and NF0.

By virtue of the fluorination treatment on the MO channels, not only the electrical performance but also the device stability against electrical, thermal, and illumination stresses is remarkably enhanced. Fig. 5 plots the threshold voltage shifts (ΔV_{th}) of Devices F1 and F0 as a function of stress time. Since Device F0 before the PLN process (i.e., Device M) is always short-circuited, its ΔV_{th} result is presented together. No matter whether a positive gate bias (thermal) stress (PB(T)S, $V_{stress}=V_{th}+20$ V, at a temperature of 85 °C) or a negative gate bias (illumination) stress (NB(I)S, $V_{stress}=V_{th}-20$ V, under white light exposure with a density of 3.6 mW/cm^2) is applied to these devices, the ones after the PLN process always show a smaller ΔV_{th} than their counterparts before the PLN process. The negative ΔV_{th} after PB(T)S is presumably attributed to the electric-field-indued donation of extra electrons by H_2O molecules and OH groups from the ESL to the AC layer [11]. Such a degradation may fade away by further improving the quality of the ESL. Device NF0 has a smaller NBIS-induced ΔV_{th} than Device F0 though the annealing steps before the PLN process has been deleted in its process flow for a reduced thermal budget. This is plausibly because the elimination of thermal annealing may allow more oxygen-related deficiency (such as oxygen vacancy) sites to be passivated by fluorine rather than oxygen. Since the formed metal-fluorine bonds (e.g, 516 kJ/mol or 5.327 eV for In-F) have much higher bond-dissociation energies than metal-oxygen bonds (e.g, 346 kJ/mol or 3.586 eV for In-O) [12], the fluorinated MO TFTs are more immune to the applied stress. These results reflect that the PLN process can be used as an efficient fluorination method to enhance device performance and stability.

Different from other fluorination methods, such as F-containing plasma treatment [7][13], our method is carried out under mild conditions, so it protects the devices from processing damage, leading to a substantially steep SS. Meanwhile, there is also no need to spare extra processes for the execution of our method, simplifying the fabrication of AM-FPD panels for a shorter production cycle and a lower process thermal budget.

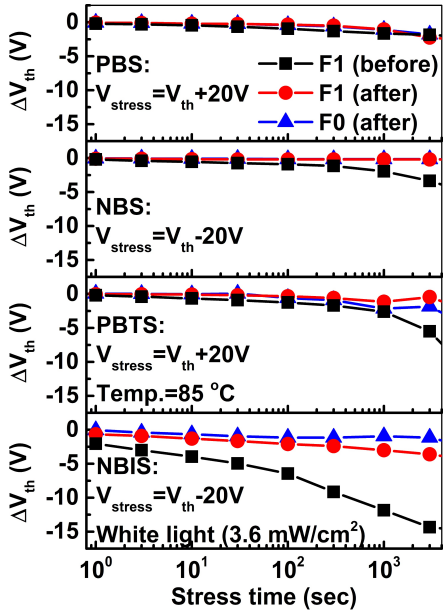

Figure 5. Plot of PB(T)S- and NB(I)S-induced ΔV_{th} as a function of stress time. The result of Device F0 before the PLN process is not shown here due to short circuit.

4. Conclusion

In this work, we utilized a fluorinated polyimide in the final PLN process as a fluorine source for enhancing the electrical performance of bottom-gated MO TFTs without the need for additional facility costs or increased thermal budget. The underlying mechanism is attributed to the diffusion of fluorine species from the PLN layer to the AC layer and the following passivation of oxygen-related deficiencies during the thermal curing of the F-PI. By adopting the fluorinated PLN layer, bottom-gated devices exhibited significantly enhanced electrical characteristics and stability. This study provides a useful method for the cost-effective production of AM-FPD panels and the implementation of MO TFTs on flexible substrates.

5. Acknowledgments

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